MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1455

TIMING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

TIMING CIRCUIT

The MC1455 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE555 Timers
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output

FIGURE 1 — 22-SECOND SOLID-STATE TIME DELAY RELAY CIRCUIT

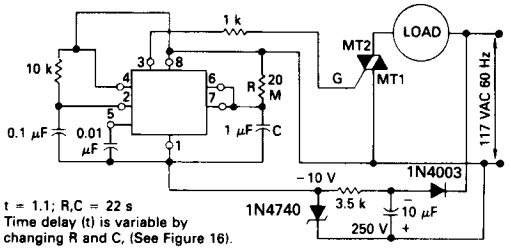
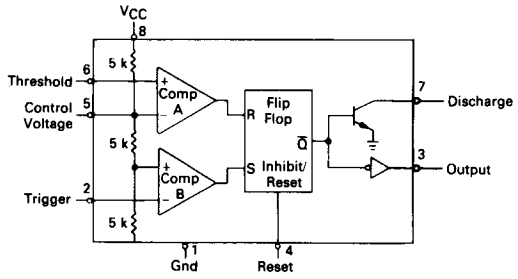


FIGURE 2 — BLOCK DIAGRAM

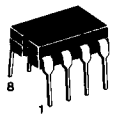


G SUFFIX
METAL PACKAGE
CASE 601

1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

P1 SUFFIX
PLASTIC PACKAGE
CASE 626

U SUFFIX
CERAMIC PACKAGE
CASE 693



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

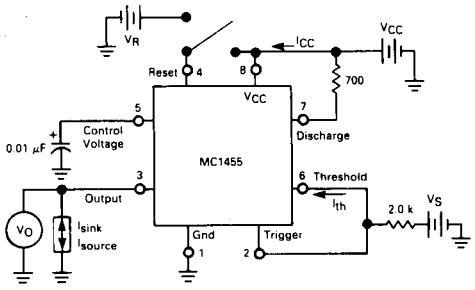
ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1455G	—	0°C to +70°C	Metal Can
MC1455P1	NE555V		Plastic DIP
MC1455D	—		SO-8
MC1455U	—		Ceramic DIP
MC1455BP1	—	−40°C to +85°C	Plastic DIP

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current (Pin 7)	I_7	200	mA
Power Dissipation (Package Limitation) Metal Can Derate above T_A = +25°C Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 680 4.6 625 5.0	 mW mW/°C mW mW/°C
Operating Temperature Range (Ambient) MC1455B MC1455	T_A	 −40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

FIGURE 3 — GENERAL TEST CIRCUIT



Test Circuit for Measuring dc Parameters: (to set output and measure parameters)
a) When V_S = 2/3 V_{CC}, V_O is low.
b) When V_S = 1/3 V_{CC}, V_O is high.
c) When V_O is low, pin 7 sinks current. To test for Reset, set V_O high, apply Reset voltage, and test for current flowing into pin 7. When Reset is not in use, it should be tied to V_{CC}.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +15 V unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage Range	V_{CC}	4.5	—	16	V
Supply Current V_{CC} = 5.0 V, R_L = ∞ V_{CC} = 15 V, R_L = ∞ Low State, (Note 1)	I_{CC}	 — —	 3.0 10	 6.0 15	mA
Timing Error (Note 2) R = 1.0 kΩ to 100 kΩ Initial Accuracy C = 0.1 μF Drift with Temperature Drift with Supply Voltage		 — — —	 1.0 50 0.1	 — — —	 % PPM/°C %/Volt
Threshold Voltage	V_{th}	—	2/3	—	xV_{CC}
Trigger Voltage V_{CC} = 15 V V_{CC} = 5.0 V	V_T	 — —	 5.0 1.67	 — —	V
Trigger Current	I_T	—	0.5	—	μA
Reset Voltage	V_R	0.4	0.7	1.0	V
Reset Current	I_R	—	0.1	—	mA
Threshold Current (Note 3)	I_{th}	—	0.1	0.25	μA
Discharge Leakage Current (Pin 7)	I_{dis}	—	—	100	nA
Control Voltage Level V_{CC} = 15 V V_{CC} = 5.0 V	V_{CL}	 9.0 2.6	 10 3.33	 11 4.0	V
Output Voltage Low (V_{CC} = 15 V) I_{sink} = 10 mA I_{sink} = 50 mA I_{sink} = 100 mA I_{sink} = 200 mA (V_{CC} = 5.0 V) I_{sink} = 8.0 mA I_{sink} = 5.0 mA	V_{OL}	 — — — — — —	 0.1 0.4 2.0 2.5 — 0.25	 0.25 0.75 2.5 — — 0.35	V
Output Voltage High (I_{source} = 200 mA) V_{CC} = 15 V (I_{source} = 100 mA) V_{CC} = 15 V V_{CC} = 5.0 V	V_{OH}	 — 12.75 2.75	 12.5 13.3 3.3	 — — —	V
Rise Time of Output	t_{OLH}	—	100	—	ns
Fall Time of Output	t_{OHL}	—	100	—	ns

NOTES:
1. Supply current when output is high is typically 1.0 mA less.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
   Monostable mode
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 megohms.

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TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 4 — TRIGGER PULSE WIDTH

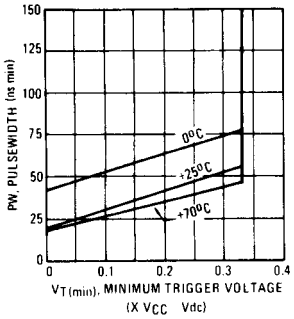


FIGURE 5 — SUPPLY CURRENT

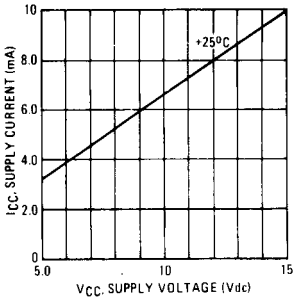


FIGURE 6 — HIGH OUTPUT VOLTAGE

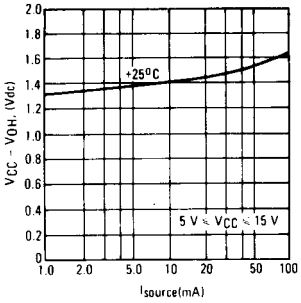


FIGURE 7 — LOW OUTPUT VOLTAGE @ V_{CC} = 5.0 Vdc

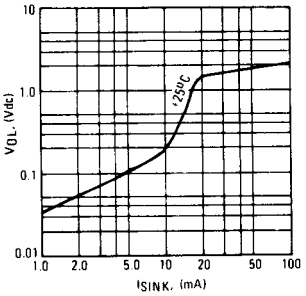


FIGURE 8 — LOW OUTPUT VOLTAGE @ V_{CC} = 10 Vdc

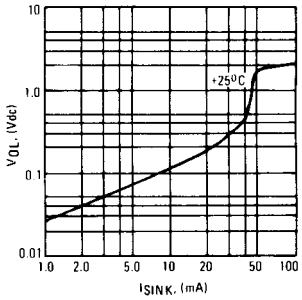


FIGURE 9 — LOW OUTPUT VOLTAGE @ V_{CC} = 15 Vdc

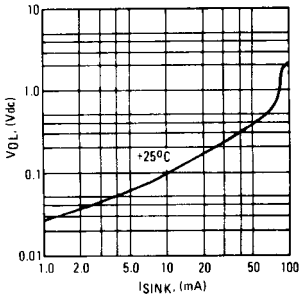


FIGURE 10 — DELAY TIME versus SUPPLY VOLTAGE

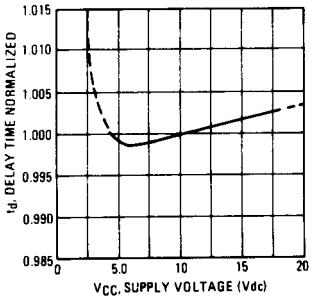


FIGURE 11 — DELAY TIME versus TEMPERATURE

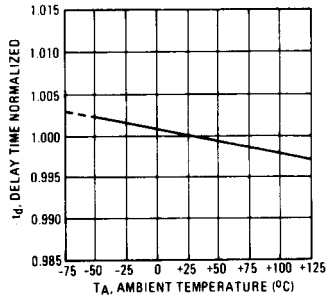
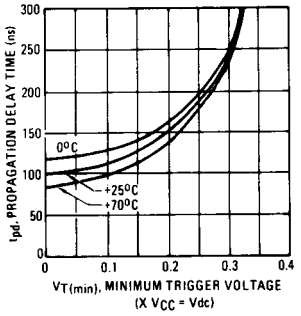
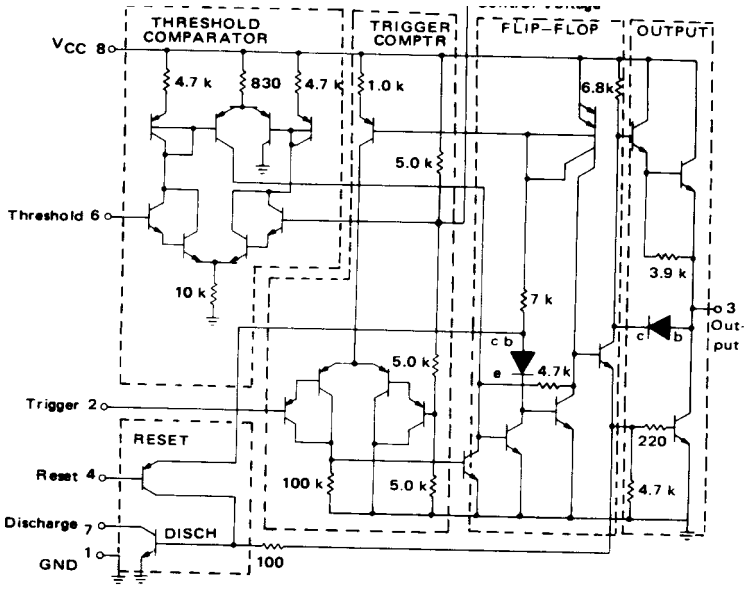


FIGURE 12 — PROPAGATION DELAY versus TRIGGER VOLTAGE





GENERAL OPERATION

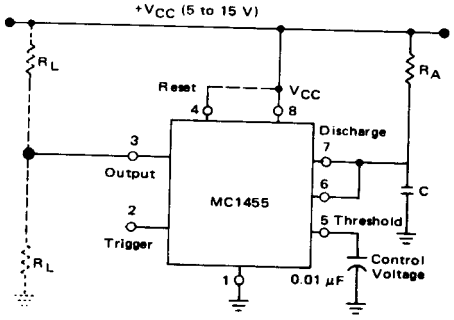
The MC1455 is a monolithic timing circuit which uses as its timing elements an external resistor — capacitor network. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below 1/3 V_{CC} the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V_{CC} the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

FIGURE 14 — MONOSTABLE CIRCUIT



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